Élan Am386SC300 Device Board Layout Suggestions

Application Note

Advanced Micro Devices

The following suggestions concern the Élan board layout strategy for the 32-kHz oscillator, the PLLs, and the power supplies.The goal is to minimize noise and noise coupling associated with the way the board is laid out. Special care is needed to minimize board leakages which can be fatal to pins that are sensitive to leakage currents, such as the two crystal oscillator pins, XTAl1 and XTAL2.

32-KHZ OSCILLATOR

Prudent board layout for the 32-kHz oscillator suggests the following precautions:

- Keep the two traces, XTAL1 and XTAL2, as short as possible, especially the input trace, XTAL1. XTAL1 is extremely sensitive to leakage. Total leakage from/to XTAL1 to/from all the pins on the board must be kept under 300 nA. XTAL2 can tolerate a leakage as high as 900 nA.
- Keep all noisy signals (e.g., PLL outputs and other clocking signals) as far away from XTAL1 and XTAL2 as possible. Again, XTAL1 is much more sensitive to noise coupling than XTAL2.
- Minimize parasitic capacitance between XTAL1 and XTAL2; even a few picofarads can potentially cause the oscillation frequency to be off target.
- Do not use a feedback resistor larger than 20 MΩ; it may fail to start up if the leakage at XTAL1 is equivalent to 5MΩ or less. The feedback resistor value can be lowered to counter leakage at XTAL1, but that will increase startup time. The lower bound for the feedback resistor should be about 10 MΩ.
- The capacitors connected between XTAL1, XTAL2, and analog ground should be between 15 pF and 30 pF, and they should be about equal in value. Increasing the two capacitor values increases startup time and power consumption, but it does reduce noise coupling into XTAL1 and XTAL2.

PHASE-LOCKED LOOPS

Board layout considerations for the four PLLs suggest the following precautions:

- Keep the output traces for the four PLLs as short as possible and keep them as far away from each other (and other clocking signals) as possible.
- Do not exceed the specified AC loading for the four PLL outputs. Certainly no DC loading is allowed since they are all CMOS logic outputs. If the PLLs have to drive more load than they are designed for in the actual application, make sure they are properly buffered on the board.

POWER SUPPLIES

Board layout considerations for the power supplies suggest the following precautions:

- Bring the analog VCC and digital VCC on separate traces from the output of the voltage regulator to the Elan device; making sure the traces are thick and wide. Filter the analog VCC with an RLC second-order low-pass filter (e.g., R= 10 Ω, L=47 μH, C=33 μF). Since the digital VCC carries much more current than the analog VCC, a second order LC low-pass filter should be used instead (i.e., The series resistor should be removed). A small capacitor in the order of a few nanofarads can be added in parallel to the large filter capacitor to suppress high-frequency noise.
- Isolate the analog ground plane from the digital ground plane on the board, and connect them after decoupling.

Issue Date: **September 1995**